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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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COMPONENT PACKAGING

The present invention relates to component packaging and finds particular application in wafer-level packaging of, for example, electrical and/or optical components such as lasers and associated devices.

Component packaging is used in semiconductor-based technologies generally to protect or support a component or an assembly of components for handling or further processing. Packaging can potentially be done at different levels, from individual items up to finished assemblies. For instance, a sub-assembly of components can be packaged together so that a function of the sub-assembly can be tested without waiting for the finished equipment.

Various types of protection can be offered by packaging, including mechanical and chemical. For example, a passivation layer can be used to provide environmental protection for any active and passive components integrated on a substrate. Such a passivation layer can be provided during an assembly process, as an intermediate layer of a wafer level assembly, or deposited as a final step in wafer level processing.

Wafer level packaging is becoming known as an attractive method of packaging low to mid density devices for several reasons: cost, size and ease of testing.

Cost is the largest force driving wafer-level packaging. Using simultaneous batch integration processing, an entire wafer or substrate can be packaged instead of packaging each device. Wafer level packaging reduces the number of steps involved in packaging, potentially eliminates the use of underfill and allows for centralized processing during fabrication. Further, packaging of the wafer allows for a high degree of process integration, due to the use of technologies such as thin film and lithography, which decreases cost. Centralized packaging during fabrication also reduces packaging time and inventory, since devices are no longer packaged separately prior to assembly.

Device size is also a driving force for wafer-level packaging. The size of a wafer level packaged device can be much the same as packaged semiconductor chips.

From the testing point of view, wafer-level packaging has a major advantage. Testing at the wafer-level (which is intermediate testing of the device functionality to decide which particular devices are going to be finally packaged and used as an end product) can reduce test costs by as much as 50%, requiring both less capital and reducing the number of test steps.

However, known wafer-level packaging is not suitable for use in the fabrication, assembly and packaging of all components and devices. For example, it is not used for active optical devices and components such as tunable and/or external cavity lasers.

Conventional approaches for wafer level integration and the fabrication of "build-up layers" on an integration substrate are based on the deposition and patterning of organic materials such as Dow Chemical's SilK, or the chemical vapour deposition (CVD) of metal oxide type coatings.

A known problem of purely organic materials is that their co-efficient of thermal expansion (CTE) is high compared to that of materials such as metals and semiconductors used in substrate-based integration for example for interconnects and other aspects of optoelectronic operations. A typical CTE of organic materials is 60 ppm (parts per million per °C) or higher. A significant mismatch in CTE between a layer and material it is in contact with tends to cause stresses at the interface. In addition, organic materials lack thermal stability, which may limit a device's long-term stability and exclude some manufacturing techniques such as soldering and metallization.

On the other hand, CVD is a high temperature process, which limits the selection of substrate materials and the type of electronic or optoelectronic devices which can be assembled to the substrate before CVD inorganic film deposition. Furthermore, the processing of openings (assembly holes) is time consuming and deep structures are relatively complicated to fabricate.

According to a first aspect of the present invention, there is provided a substrate-based assembly for carrying optical and/or electrical components, the substrate-based assembly comprising a packaging layer, wherein the packaging layer comprises a glass material having both organic and inorganic components.

The "substrate-based assembly" may comprise a wafer assembly in which at least one device or component is to be supported on a wafer of material as substrate. A "substrate-based assembly" might already have a device or component mounted thereon but the phrase encompasses a substrate plus packaging layer prior to, or in the absence of, mounting of any device or component.

A "glass material" in this context is used in the usual way to mean an amorphous or non-crystalline solid. References elsewhere in this description to a "hybrid glass material" and the like are intended to refer to a glass material having both inorganic and organic components.

In an embodiment of the present invention, because of its organic/inorganic nature, it is possible to select a glass material for the packaging layer which has one or more particular properties. For example, the adjustment of the organic/inorganic ratio makes it possible to tune the values for one or more of: CTE; hardness; stress modulus (known as substrate bow); and thermal stability.

For example, if the concentration of inorganic materials is increased:

- the CTE decreases
- the hardness increases
- the stress modulus increases
- thermal stability typically increases.

If the concentration of organic materials is increased:

- the material softens and becomes more elastic
- the CTE increases
- the thermal stability decreases.

The CTE of suitable organic materials is typically 50 ppm or more and the CTE of inorganic materials (e.g. glass, silica, alumina etc.) is typically just a few ppm or less. Hence it is available to tune the CTE over a significant range by adjusting the inorganic/organic ratio in the material. For example, the CTE is 100 ppm or more in materials having an epoxy concentration of about 70% or more while alumina has a CTE of 6.7 ppm and silica has a CTE of 0.5 ppm.

A substrate-based assembly according to the first aspect of the present invention may further comprise electrical interconnect material.

It will usually be preferable that the value of the CTE for the hybrid glass material used as a packaging layer approaches that of the electrical interconnect material. For example, suitable interconnect materials that might be used are copper and aluminium, in which case the closer the CTE of the hybrid glass material is to the values for copper and aluminium the better. In general, it is preferable that the CTE of the hybrid glass material should not differ more than 15 ppm from the CTE of the interconnect material.

It may also or instead be preferred that the value of the CTE for the hybrid glass material used as a packaging layer approaches that of the substrate material. For example, it might be

preferred that the CTE of the hybrid glass material should not differ more than 15 or 20 ppm from the CTE of the substrate material.

The electrical interconnect material might be present for example as structures such as contact pads for bump bonding or for wire bonding. A sub-assembly comprising an embodiment of the present invention may be used as an integration level for bump bonding in which a bump of conductive material is positioned on a pad of interconnect material, or indeed double bump bonding where a double layer of solders (bumps) is created on top of interconnect material that has been provided in the sub-assembly.

Concentration levels of inorganic and organic material components can be varied considerably in the glass material, providing a potential range of CTE values for example from 3 to 100 ppm. In the glass material, an inorganic matrix can be provided at least in part by any metal alkoxide or salt that can be hydrolysed, all of these being appropriate inorganic network formers, including those based on groups 3A, 3B, 4B and 5B of the Periodic Table, such as silicon dioxide, aluminium oxide, titanium dioxide and zirconium oxide.

Functional organic moieties can then be used to modify the inorganic matrix. In general, the glass material of the substrate-based assembly will preferably include an organic component which polymerises by cross-linking. It might for instance be an organic component which polymerises under thermal or photo treatment, such as the functional hydrocarbon compounds comprising acrylates, epoxides, alkyls, alkenes, or aromatic groups which support photopolymerisation.

The hybrid glass material of the packaging layer in a substrate-based assembly according to the first aspect of the present invention may advantageously have lithographic properties. The combination of organic and inorganic properties allows direct photolithographic patterning of the glass material. Thus it can be possible to select materials in embodiments of the present invention such that all fabricated structures can be produced by lithographic processing. This enables accurate positioning (sub micrometer accuracy) of components such as optical sub-assembly elements. Electrical interconnects can be created either before or after deposition of the hybrid glass material and the components can be mounted after the patterning of the hybrid glass material.

For example, the packaging layer of a substrate-based assembly according to the first aspect of the present invention might be provided with recesses during patterning, either as depressions or holes, in relation to which one or more components can subsequently be mounted.

All the inorganic and organic material components mentioned above are very favourable in terms of their properties and their tunability for wafer-scale integration.

By selection of appropriate components, it is possible to use low temperature processing of a hybrid glass material, for instance at less than 450 °C or even less than 200 °C or even 150 °C. This makes it possible to integrate the glass onto existing electronic components and circuitry. In particular, if high processing temperatures are required the organic component content should be kept to a minimum. Low processing temperatures are made possible by using thermal- or photoinitiators resulting in polymerization of the organic matrix. The polymerisation may be achieved through organic carbon-carbon double bond openings and crosslinking. Known thermal initiators include benzophenone and various peroxides, such as benzoylperoxide and layroyl peroxide. Known photoinitiators include phenyl bis(2,4,6-trimethylbenzoyl)phosphine oxide (Irgacure 819) and 1-hydroxy-cyclohexyl-phenyl-ketone (Irgacure 814). (Irgacure initiators are products of Ciba Specialty Chemicals Inc. and "Irgacure" is a registered trade mark.)

In a novel arrangement, one or more components may be mounted in the substrate-based assembly for electrical interconnection using the known technique of "solder bump bonding". Standard solders such as lead and tin alloys can be used. In this known technique, solder bumps are applied to a connection surface of the component, or to a support surface, the component is placed in contact via the bumps with the support surface and then heat is applied. The solder flows to provide a relatively intimate bond and good electrical performance in use. Solder bump bonding has not been used in packaging discrete optical components in the past. It has been found to have a very significant advantage however in that the components can be accurately aligned by manipulation while the bonding material is soft. This can be done during a mounting operation or subsequently by applying heat to the bonding material.

As well as components or devices, the substrate may also or instead support control electronics such as laser drivers, thermo-elements, signal controllers, buried integrated circuits such as central processing units (CPUs) for embedded software, and their various interconnects. One substrate can carry one to several tens of sub-assembly structures.

Suitable substrates for use in embodiments of the present invention are silicon, glass, composite materials, ceramics including multi-layer ceramics such as alumina and low temperature-co-fired ceramics (LTTC), and even conventional printed circuit board.

The packaging layer might be supported directly or indirectly by the substrate. One potential use for a packaging layer comprising a hybrid glass material is as a passivation layer and this might be applied during, or as a final layer in, wafer processing.

Optoelectronic equipment comprising a substrate-based assembly according to an embodiment of the present invention is also encompassed as an embodiment of the present invention. For example, this might be an optical source such as a wavelength tunable optical source.

A packaging layer in a substrate-based assembly according to an embodiment of the present invention may be used to transmit optical radiation in use of the assembly, in which case the optical properties of the material of the packaging layer will be important. It may be preferred that more than one packaging layer is provided, each packaging layer comprising a glass material having both organic and inorganic components. Where the assembly is to be used to carry optical radiation, it may be preferred that the packaging layers have differing optical qualities. For example, if one packaging layer has a different refractive index from another packaging layer, this might be used to support confinement of the optical radiation as it travels through the assembly.

According to a second aspect of the present invention, there is provided a method of packaging a substrate-based assembly, which method comprises the step of providing a packaging layer comprising a glass material having both organic and inorganic components.

A method according to the second aspect of the present invention may optionally comprise the step of providing one or more electrical interconnect structures in or adjacent to the packaging layer.

Further, such a method may include the step of using bump bonding to bond a component to an electrical interconnect structure. This has the advantage that the method may further comprise final alignment of two or more components by manipulating at least one of the components while the bonding material is sufficiently soft to accommodate the manipulation. For instance, the method might comprise the steps of:

a) maintaining the temperature of the bump bonding material above a softening temperature for the material and micro-manipulating the component in relation to the mounting pad; and

b) lowering the temperature of the bump bonding material to below said softening temperature so as to achieve bump bonding.

A method according to the second aspect of the present invention may optionally comprise the step of lithographic processing of the packaging layer. Such lithographic processing might be used for example to provide one or more recesses or holes in the packaging layer for use in positioning one or more components of the substrate-based assembly. Advantageously, embodiments of the present invention will support a method of fabricating a substrate-based assembly which method comprises lithographic processing of each fabricated layer of the substrate-based assembly. This offers very accurate positioning of components.

Further, a method according to the second aspect of the present invention may optionally comprise the step of using gray scale lithography to fabricate a groove of tapered cross section in a packaging layer for mounting a fibre for optical coupling with an optical component.

Embodiments of the present invention can provide a practicable wafer-level packaging technique for electrical and/or optical components. In particular, embodiments of the invention can provide a novel method to fabricate an optical sub assembly at wafer-level, followed by alignment, testing and chip-scale packaging of the sub assembly.

Embodiments of the present invention are useful in packaging active (i.e. gain providing) optical devices. As an example, an embodiment of the invention can be used to manufacture chip-scale packaged tunable laser components. However, embodiments of the invention are not limited to use in packaging optical components but can be applied in packaging various electrical and optoelectrical devices. Resulting devices can be very compact and free of electromagnetic interference (EMI) and vibrational problems. Ease of integration and testing reduces device cost dramatically due to reducing the required equipment capital as well as ease of testing and early failure detection. In addition, due to the compact size and fairly dense integration level, resulting devices are reliable and can be used for example in modulation as very fast optoelectrical devices.

A process for wafer level packaging will now be described as an embodiment of the present invention, by way of example only, with reference to the accompanying figures in which:

Figure 1 shows a schematic three quarter view of a substrate for use in fabricating wafer assemblies;

Figure 2 shows the substrate of Figure 1 with a packaging layer deposited on the substrate;

Figure 3 shows the substrate of Figure 2 after lithographic processing of the packaging layer to produce multiple patterned structures;

Figure 4 shows the structure of Figure 3 after addition of a spin-on glass layer above the patterned structures of the packaging layer;

Figure 5 shows one of the patterned structures of Figure 3 in more detail;

Figure 6 shows the patterned structure of Figure 5 with the supporting substrate and the spin-on glass layer;

Figure 7 shows a vertical cross section through the patterned structure and supporting substrate of Figure 6, generally along the optical axis of the sub-assembly which the structure is intended to accommodate;

Figure 8 shows a plan view, from above, of a first ("closed") version of the patterned structure of Figure 5;

Figure 9 shows a plan view, from above, of a second ("open") version of the patterned structure of Figure 5;

Figure 10 shows the same vertical cross section as that shown in Figure 7 with the addition of a wire-bonded sub-assembly of components which the structure is intended to accommodate. Both Figures 10A and 10B show a "closed" patterned structure, as shown in Figure 8;

Figure 11 shows a three quarter view from above of the wire-bonded sub-assembly shown in Figure 10, in place in the wafer sub-assembly;

Figure 12 shows the vertical cross section of Figure 7 with the addition of a bump-bonded sub-assembly of components which the structure is intended to accommodate;

Figure 13 indicates degrees of freedom in micromanipulation for alignment of optical components during fabrication of a wafer sub-assembly;

Figure 14 shows a contact pad in cross section, for use in a bump-bonded sub-assembly as shown in Figure 12; and

Figure 15 shows a joining structure for a fibre pigtail in cross section, for use in a bump-bonded sub-assembly as shown in Figure 12.

It should be noted that none of the figures is intended to be drawn to scale. The figures are schematic representations only.

Referring to Figure 1, a substrate 100 suitable for use in integrating active and/or passive components and devices might comprise silicon (CTE = 3 ppm), glass (CTE = 8 ppm), composite materials, ceramics including multi-layer ceramics such as alumina (CTE = 6 ppm), and low temperature-co-fired ceramics (LTTC), and even conventional printed circuit board materials such as polyimide (CTE = 50 ppm) and FR-4 (CTE = 16 ppm). The dimensions of the substrate 100 might vary considerably, for instance having dimensions of the order of less than one inch up to about twelve inches. In the following example, the substrate is a pre-fabricated, six-inch substrate.

Referring to Figure 2, a packaging layer 200 of hybrid glass material is applied to the whole substrate and pre-baked before patterning by exposure using ultra-violet (UV) light. The layer thickness may vary from 1 nm to 1 mm.

Example 1

In more detail, in a first method the packaging layer 200 of hybrid glass material (CTE approximately 35 ppm) is synthesized by applying wet chemistry processing techniques (ie synthesis using liquid phase conditions). In particular, 0.1 mol of 3-glysidoxy-propyl trimethoxysilane is mixed with 0.0125 mol of tetrachlorosilane in excess of diethyl chloride. The solution is refluxed and then 0.1 mol of 3-methacryloxy-propyl trimethoxysilane and 0.05 mol of tetrachlorosilane are added to the solution. In addition, excess of ultra pure water (typically where contamination is less than 10 ppb) is added and the mixture is allowed to react for several hours. Sodium hydrocarbonate is added into the solution after which the precipitate is filtered. The material is finalized by removing volatile components such as water and solvent from the solution and 0.5 w-% of benzophenone and 0.25 w-% of Irgacure 819 are added.

The following lists the purposes of each of the precursors mentioned above although it should be noted that they may be multi functional:

3-Glysidoxy-propyl trimethoxysilane

is used to increase the CTE and produce flexibility in the matrix. The glysidoxy part of the molecule may also be used for thermal or photo polymerisation of the material. The trimethoxy part of the precursor undergoes a hydrolysis and condensation reaction and forms a silicon oxide matrix. It thus decreases the CTE but increases the thermal stability.

Tetrachlorosilane

undergoes hydrolysis and condensation and contributes to a silicon dioxide matrix in the material system. It increases thermal stability and decreases CTE. It may also be used as a catalyst for the ring-opening polymerisation of the epoxy (e.g. glysidoxy) moieties in the material since it acts as a Lewis acid.

3-Methacryloxy propyl trimethoxysilane

is used to create photosensitivity in the material. A methacryloxy moiety forms the photosensitivity through acryloxy carbon to carbon double bond breakage and continual crosslinking polymerisation. The organic polymer matrix formed increases the CTE and is not

as stable as an inorganic silicon oxide matrix. The trimethoxy part undergoes hydrolysis and condensation and forms a silicon oxide matrix.

Water

is used as a hydrolyzation agent for alkoxides and chlorates.

Sodium hydrocarbonate

is used to neutralize the material which contains some free chlorine ions. The carbonate reacts with free protons and thus neutralizes the solution.

Benzophenone

is used as a thermal/photo initiator to form free radicals during thermal/photo exposure to create methacryloxy crosslinking.

Irgacure

is used as a photoinitiator to form free radicals during photo exposure to activate methacryloxy crosslinking. Irgacure is a product of Ciba Specialty Chemicals.

The material is spun-on (or alternatively dip deposited) by applying a dynamic spinning procedure. Edge bead removal is carried out by using acetone spray. The sample is prebaked at 120 °C for 5 minutes on a hot plate in nitrogen.

Example 2

In a second method, the packaging layer 200 of hybrid glass material (CTE approximately 15 ppm) is synthesized as follows. 0.1 mol of phenyltrichlorosilane, 0.1 of 3-methacryloxypropyl trichlorosilane and 0.016 mol of trimethylolpropane trimethacrylate are mixed and hydrolysed in the presence of dichloromethane and ultra pure water. The mixture is reacted for a time (from 1 hour to 48 hours) sufficient to allow all the silanes to hydrolyze. The organic solvent phase is separated from the solution. The material is finalized by removing volatile components such as water and solvent from the solution and 0.5 w-% of benzophenone and 0.25 w-% of Irgacure 819 and Irgacure 184 are added.

In this second method:

Phenyltrichlorosilane

is used to increases the CTE from silicon dioxide values. The phenyl moiety is highly stable and also provides physical flexibility and elasticity in the resulting material. It hydrolyses and condenses to form a silicon oxide matrix.

3-methacryloxypropyltrichlorosilane

is used to create photosensitivity in the material. A methacryloxy moiety forms the photosensitivity through acryloxy carbon to carbon double bond breakage and continual crosslinking polymerisation. The organic polymer matrix formed increases the CTE and is not as stable as an inorganic silicon oxide matrix. The trichloro part undergoes hydrolysis and condensation and forms a silicon oxide matrix.

Trimethylolpropane trimethacrylate

is used to increase the photosensitivity of the material during exposure. The three methacryloxy moieties in the molecule participate in the free radical polymerisation and result in a highly crosslinked organic matrix. The organic polymer matrix formed increases the CTE and is not as stable as an inorganic silicon oxide matrix.

Benzophenone

is used as a thermal/photo initiator to form free radicals during thermal/optical exposure to create methacryloxy crosslinking.

Irgacure

is used as a photoinitiator to form free radicals during photo exposure to activate methacryloxy crosslinking. Irgacure is a product of Ciba Specialty Chemicals.

The material is spun-on (or alternatively dip deposited) by applying a dynamic spinning procedure and edge bead removal is carried out by using acetone spray. The sample is prebaked at 120 °C for 10 minutes on a hot plate in nitrogen.

Example 3

In a third method, the packaging layer 200 of glass material (CTE approximately 22 ppm) is synthesized as follows. 0.1 mol of phenyltrichlorosilane and 0.1 mol of trichlorovinylsilane are mixed and hydrolyzed in the presence of dichloromethane and ultra pure water. The mixture is reacted for a time (from 1 hour to 48 hours) sufficient to allow all the silanes to hydrolyze. The organic solvent phase is separated from the solution. The material is finalized by removing volatile components such as water and solvent from the solution and 0.5 w-% of benzophenone and 0.25 w-% of Irgacure 819 and Irgacure 184 are added.

In this third method:

Phenyltrichlorosilane
is used to increases the CTE from silicon dioxide values. The phenyl moiety is highly stable and also provides flexibility for the resulting material. It hydrolyses and condenses to form a silicon oxide matrix.

Trichlorovinylsilane
is used to create photosensitivity in the material. A vinyl moiety forms the photosensitivity through the carbon to carbon double bond breakage and continual crosslinking polymerisation. The organic polymer matrix formed increases the CTE. The organic matrix is not as stable as an inorganic silicon oxide matrix. The trichloro part undergoes hydrolysis and condensation and forms a silicon oxide matrix.

Benzophenone
is used as a thermal/photo initiator to form free radicals during thermal/photo exposure to create methacryloxy crosslinking.

Irgacure
is used as a photoinitiator to form free radicals during photo exposure to activate methacryloxy crosslinking. Irgacure is a product of Ciba Specialty Chemicals.

The material is spun-on (or alternatively dip deposited) by applying a dynamic spinning procedure and edge bead removal is carried out by using acetone spray. The sample is prebaked this time at 150 °C for 5 minutes on a hot plate in nitrogen.

As mentioned earlier in this specification, if high processing temperatures are required the organic component content of the packaging layer 200 should be kept to a minimum. Low processing temperatures are made possible by using thermal or photo initiation of the organic matrix. In Examples 1 to 3 described above, three different hybrid glass material compositions and synthesis procedures are described that can be processed at various temperatures. Material synthesized according to Example 1 requires a processing temperature of not more than 200°C. Material synthesized according to Example 2 requires a processing temperature of not more than 150°C. Material synthesized according to Example 3 allows baking temperatures up to 450°C or so. This can be particularly advantageous for example where a soldering operation is to be carried out since the materials may then be subjected to relatively high temperatures.

Referring to Figure 3, the packaging layer 200 is patterned lithographically by exposing it to UV light and developing it with a chemical developer. The layer 200 may also be treated at elevated temperature to increase the density of the glass material. The result is a plurality of patterned structures 300 which contain features for use in integration that are shown in more detail in Figures 5 to 9.

In more detail, the packaging layer 200 is UV (I-line) exposed through a dark-field contact mask which contains both binary and gray-scale features. The packaging layer 200 is then spray developed with a mixed ethanol methyl isopropyl ketone developer. The material acts as a negative-tone photoresist. This part of the process is finalized by baking at 200 °C for 2 hours in nitrogen.

Gray scale lithography, for producing gray-scale features, is a known technique described for example in the following: "Fabrication of Micro-Optical Structures by Applying Negative-Tone Hybrid Glass Materials and Greyscale Lithography", by A.H.O. Kärkkäinen, J.T. Rantala, M.R.Descour, published in Electronics Letters, Vol. 38, No. 1, pp 23-24 (2002).

The process just described can be used to produce a thick assembly structure (for instance in the range from 1 micron to 1 mm) by lithographic means. This structure might for instance have recesses or holes in which contact pads and optical and/or electrical components can be positioned in relation to one another and these are further described with reference to Figures 5 to 9.

Referring to Figure 4, once the components and interconnect material are in place, in or on the packaging layer 200, an optional further packaging layer 400 can be deposited for further protection and strength, using a spin-on glass procedure followed by processing at low temperature at wafer level. This further packaging layer 400 can again be of hybrid glass but conventional polymers such as polyimides or epoxides can also be used. Typically, the further packaging layer 400 is made of a material which is an optically different mix from that of the earlier packaging layer 200 to produce a lower refractive index in the further packaging layer 400. This lower refractive index allows the further packaging layer 400 to provide optical confinement for instance of an evanescent field associated with optical radiation travelling in the assembly in use. The thickness of the further packaging layer 400 will usually be at least 1 micron but in any event preferably thick enough that optical and/or electrical components already mounted are buried under it.

(The patterned structures are shown in dotted outline in Figure 4. However, this should not be taken to mean that the further packaging layer 400 is opaque in visible light. It may or may not be opaque in visible light.)

Referring to Figure 5, each one of the patterned structures 300 of Figure 3 is a patterned hybrid glass structure that contains a set of recesses or holes, each one of which provides an integration location for a component or other element of an assembly. For example, each recess or hole as shown in Figure 5 might be dimensioned and positioned to provide the following:

- photodetector recess 500
- gain element recess 505
- tunable reflection element recess 510
- optical isolator recess 515
- thermo element or temperature sensor recess 520
- fibre groove 525
- integration or contact pads 530

An assembly with its components in place (see Figure 10) might for example be used as a tunable optical source of the type described in US patent application No. 10/046,914 assigned to Optitune plc. In such an optical source, a tunable element 1010, such as an electro-optically controlled zone plate device or a Fabry Perot element which can be moved using a micro-electromechanical system (MEMS), is used to return optical radiation of a selected wavelength to a tunable laser 1015. A photodiode 1020 can be used to monitor the laser performance and the output of the assembly can be picked up by a fibre 1000 located in the fibre groove 525.

Other ways of tuning an optical source that might be used in an embodiment of the present invention include a tunable thin film filter, a micro-prism, a prism-grating combination or a prism-grating-prism device.

As well as the directly functional parts of an assembly as described above, it is also possible to embed control electronics such as thermal controllers, based on for example a thermo element or temperature sensor 520 which is also locatable at a hole or recess in the packaging layer 200 of the glass material. This becomes available because of the very low processing temperatures, for instance less than 200 °C, at which the hybrid glass material can be deposited. Hence the packaging layer 200 can be fabricated on top of metallic structures which typically have a melting point around 350 °C or more. Conventional glass manufacturing techniques cannot be

used in such circumstances due to the fact that they typically require temperatures of more than 800 °C to consolidate.

Another significant advantage of the hybrid glass materials as a packaging material is that conventional glass materials cannot be directly lithographically patterned after deposition. The use of a hybrid glass material which has lithographic patterning capability removes a significant number of processing steps in manufacture.

Although described primarily as being located in the packaging layer 200 as described above, control electronics can alternatively be fabricated either into the substrate 100 or on top of the substrate 100. If they are located in the hybrid glass packaging material, that might be by use of holes or recesses as described above and/or by the use of a second hybrid glass material deposition. This is shown as a further layer 400 in Figure 6.

The substrate 100 may also include optically active device such as taps (photodiodes), laser drivers and wavelength reference devices. They might be integrated inside the substrate or in layers deposited above the substrate.

Interconnect material is present in the packaging layer 200 as the integration or contact pads 530. Such interconnect material is of known type and configuration and might comprise for example copper (CTE 17 ppm) or aluminium (CTE 23 ppm). To make electrical connection, the integration or contact pads 530 can be provided on thin pads at the surface of the substrate 100 or integrated into a layer provided for the purpose. To make electrical connection between the contact pads 530 and components, wire bonds 1100 (shown in Figure 11) can be used.

In an alternative arrangement, electrically interconnecting mounting pads 1200 can be positioned in the component recesses 500, 505, 510, 515, 520 and the known technique of "solder bump bonding" can be used. This is shown in Figure 12.

In general, fabrication and connection of the mounting or contact pads 530, 1030 is further discussed below with reference to Figures 13 to 15.

After creation of the patterned hybrid glass packaging layer 200 with its mounting or contact pads 530, 1030, the layer(s) can "back" polished using a chemical and/or mechanical polishing technique. Electrical and/or optical components can then be mounted to create a wafer assembly. Such components might include for example a gain element, photodetector, reflecting element, lenses (ball or graded index type), optical isolator, and a thermo-element.

Referring to Figure 7, a cross section long the line "A-A" in Figure 6, viewed in the direction indicated by the arrows, shows lithographically defined holes in the packaging layer 200 for the following:

- photodetector hole 500
- gain element hole 505
- tunable reflection element hole 510
- optical isolator hole 515

The fibre V-groove 525 is also shown. Such a groove can be fabricated using known gray scale lithography techniques. Although shown in Figure 7 as a hole, the depth of the groove will of course be tailored to the dimensions of the fibre end to be located therein and might be for instance of the order of 50 μm deep.

Referring to Figures 8 and 9, the patterned packaging layer may be provided with a "closed" integration structure, as shown in Figure 8, or an "open" integration structure, as shown in Figure 9. That is, the holes or recesses for the various components might be designed as physically discrete and separate features in the packaging layer 200 or they may be interconnected.

A primary difference between the closed and open structures in practice is the presence or absence of the packaging layer 200 in the optical transmission path through the components. In the closed structure, if the packaging layer 200 is deep enough, it will lie in at least part of the optical transmission path between the components. This can be understood particularly with reference to Figures 10A and 10B which show components 1020, 1015, 1010, 1005 located in appropriate holes in the packaging layer 200. In Figure 10A, the components are all aligned along a common optical axis 1025 but the optical axis lies above the packaging layer 200 and the optical transmission path of the assembly does not pass through any part of the packaging layer 200. In a closed structure as shown in Figure 8, if the packaging layer 200 were deeper relative to the components, the common optical axis 1025 would pass through it. This has implications for the choice of packaging layer material since optical properties such as transparency and refractive index could become important. Such a configuration is shown in Figure 10B.

Referring to Figure 10 , this shows a cross section similar to that of Figure 7 but with components located to their appropriate holes in the packaging layer 200. In particular, the following components can be seen located:

- photodetector 1020
- gain element 1015
- tunable reflection element 1010
- optical isolator 1005
- single mode optical fibre 1000

These components 1000, 1005, 1010, 1015, 1020 are mounted on integration pads 1030 and aligned along a common optical axis 1025 which lies above the packaging layer 200. The packaging layer 200 might thus be deposited as a closed structure regardless of its optical characteristics, as shown in Figure 8, although it may have for example guiding or absorption characteristics which need to be taken into account in use. The closed structure has an advantage in providing improved protection to the substrate in comparison with an open structure as shown in Figure 9. The packaging layer 200 can provide at least coarse alignment of the optical components as well as mechanical protection.

The integration pads 1030 are constructed from any suitable material which will adhere to the components and other materials it will be in contact with. The pads 1030 may or may not be electrically conductive, as required.

In Figure 10A, both a gain element 1015 and a separate tunable reflection element 1010 are shown. These can be used together to provide a tunable optical source. The gain element 1015 might be an external cavity, single mode semiconductor laser whose output can be tuned by tuning the feedback from an external cavity created by the tunable reflection element 1010. For example, the tunable reflection element 1010 might comprise a diffraction device arranged in a Littrow configuration, the diffraction device comprising a thermo-optic material which can be thermally controlled for tuning.

In practice, the tunable reflection element 1010 might be replaced or supplemented by the use of an external optical modulator such as an amplitude, frequency and/or intensity modulator. More specifically, for example, an external modulator might be a Mach-Zehnder modulator, a semiconductor multiple quantum well modulator or an electrorefraction modulator.

Referring to Figure 10B, the gain element 1015 and separate tunable reflection element 1010 might be replaced by a monolithic tunable source 1035 such as that disclosed in US patent 6041071 in the name Coretek Inc, or that disclosed in US patent 6275317 in the name Agere Systems Optoclectronics Guardian Corp. Another example of an integrated form of tunable

source 1035 is disclosed in copending US patent application 10/046,914 assigned to Optitune PLC.

Referring to Figure 11, metallic interconnect pads 530 are also positioned in holes in the packaging layer 200. These contact pads 530 may be made of metals known to be suitable for bonding using wire bonding. Electrical connection to the components 1000, 1005, 1010, 1015 can then be provided as necessary using wire bonds 1100.

The components 1000, 1005, 1010, 1015 can largely be mounted and the wire bonds 1100 put in place before a wafer assembly is diced into individual assemblies. It is only generally possible to mount the fibre 1000 to its groove after dicing however.

Referring to Figure 12, instead of using wire bonds 1100 the components 1000, 1005, 1010, 1015 can be mounted using the known technique of "solder bump bonding". In this technique, electrical interconnection is provided by mounting pads 1200 in the holes in the packaging layer 200 under the components. The components 1000, 1005, 1010, 1015 are provided with solder bumps 1205 on their bonding surface and these solder bumps 1205 are brought into contact with the interconnecting mounting pads 1200 and heated to form a bond between the component and the mounting pad 1200. After the heat treatment, the solder bumps are spread into intimate contact with the components 1000, 1005, 1010, 1015 and the mounting pads 1200 and can provide particularly good electrical performance.

There are variations in solder bump bonding which can also be used in an embodiment of the present invention. For example the solder bumps 1205 can be provided on interconnect material in the mounting pads 1200 instead of or as well as on a bonding surface of the components. In "double bump bonding", two layers of bumps are provided, one on top of the other.

The electrical contact pads 530 and interconnecting mounting pads 1200 can be fabricated by post-processing of the substrate 100 and packaging layer 200 and this is further discussed below with reference to Figures 13 to 15.

The use of bump bonding provides thermo-mechanical as well as environmental protection for interconnects in the sub assembly layer. Optical components attached using the bumps are protected from shear stresses. Furthermore, this technique eliminates use of an underfill process which might otherwise be necessary for die or component attachment, which makes the processing procedures less complicated.

In practice, the use of the solder bumps 1205 and mounting pads 1200 also makes it possible to tune the positioning of optical components even after they are bonded to electrical interconnect material. The bonding material can be slightly heated so that it softens to accommodate movement of the components, for instance on a hot chuck or by using a laser or the like. Movements of a few hundred nanometers are possible in lateral positioning and movements of a few tens of nanometers are easily achievable in vertical position tuning without causing high stresses in the component structures.

Referring to Figure 13, an optical component such as a gain element 1015 can be mounted on a pair of contact pads 1200 by means of bump bonding. It can then be manipulated about vertical and/or horizontal planes by the use of for example a piezo or stepper motor controlled, nano-positioning stage "push" device while the solder material between the component 1015 and the contact pad 1200 is softened by the use of heat.

Referring to Figure 14, in more detail, each contact pad 1200 might be put down onto a thin film pad 1400 of a material such as solder which has been provided on or in the substrate 100. The contact pad 1200 can for example be evaporated or grown electrolytically through a window in a photoresist mask. Its dimensions might be for example 5μm x 5μm in cross section with a depth in the range 0.5 to 100 μm, depending on the required position of the component to be mounted on it. The material of the contact pad might be for example a metal such as aluminium, gold, tin, molybdenum, nickel, platinum or copper but it may contain more than one layer and more than one material. The contact pad 1200 of Figure 14 shows three layers.

Referring to Figure 15, another type of structure which might require to be mounted is a joining structure 1505 for a fibre pigtail (not shown). This might comprise the joining structure, mounted on a pad 1510 supported by the substrate 100. The joining structure at the same time supports a ball lens 1500. The fibre pigtail can then be mounted to abut the joining structure 1505 such that its optical axis is aligned with the lens 1500.

CLAIMS

1. A substrate-based assembly for carrying optical and/or electrical components, the substrate-based assembly comprising a packaging layer, wherein the packaging layer comprises a glass material having both organic and inorganic components.

2. A substrate-based assembly according to Claim 1 wherein the glass material includes an organic component which polymerises by cross-linking.

3. A substrate-based assembly according to either one of the preceding claims wherein the glass material includes an organic component which polymerises under thermal or photo treatment.

4. A substrate-based assembly according to any one of the preceding claims wherein the glass material includes at least one of an epoxy component, aluminium oxide and silicon oxide.

5. A substrate-based assembly according to any one of the preceding claims wherein the glass material comprises an inorganic matrix provided at least in part by a metal alkoxide or salt, the metal alkoxide or salt each being hydrolysed in provision of the inorganic matrix.

6. A substrate-based assembly according to claim 5 wherein the metal alkoxide or salt is based on groups 3A, 3B, 4B and/or 5B of the Periodic Table.

7. A substrate-based assembly according to any one of the preceding claims wherein the glass material includes at least one hydrocarbon compound from the group comprising acrylates, epoxides, alkyls, alkenes, and aromatic groups.

8. A substrate-based assembly according to any one of the preceding claims wherein the coefficient of thermal expansion of the packaging layer approaches that of the substrate material.

9. A substrate-based assembly according to any one of the preceding claims which further comprises electrical interconnect material for providing electrical connection to at least one component packaged by the packaging layer.

10. A substrate-based assembly according to Claim 9 wherein the coefficient of thermal expansion of the packaging layer approaches that of the electrical interconnect material.

11. A substrate-based assembly according to either one of Claims 8 or 10 wherein the coefficient of thermal expansion of the packaging layer differs from the coefficient of thermal expansion of the electrical interconnect material and/or the substrate material by not more than 15 parts per million.

12. A substrate-based assembly according to any one of claims 9, 10 or 11 which further comprises at least one contact pad for a wire bond to the at least one component, the electrical interconnect material being present in said contact pad or wire bond.

13. A substrate-based assembly according to any one of claims 9, 10 or 11 which further comprises at least one mounting pad for mounting the at least one component, the electrical interconnect material being present in said mounting pad.

14. A substrate-based assembly according to any one of the preceding claims, comprising a bump bonded optical component.

15. A substrate-based assembly according to any one of the preceding claims wherein the material of the packaging layer is lithographically patterned.

16. A substrate-based assembly according to Claim 15 wherein the material of the packaging layer comprises at least one organic material which photopolymerizes, the at least one organic material being selected from the group comprising acrylates, epoxides, alkyls, alkenes, and aromatic groups.

17. A substrate-based assembly according to any one of the preceding claims wherein the packaging material has a processing temperature of not more than 450°C.

18. A substrate-based assembly according to any one of the preceding claims wherein the packaging material has a processing temperature of not more than 200°C.

19. A substrate-based assembly according to any one of the preceding claims wherein the packaging material has a processing temperature of not more than 150°C.

20. A substrate-based assembly according to any one of Claims 17, 18 or 19 wherein the packaging material is fabricated from a material comprising a polymerisation initiator.

21. A substrate-based assembly according to any one of the preceding claims which comprises at least one optical component and at least one electronic device.

22. A substrate-based assembly according to Claim 21 wherein the at least one electronic device comprises an integrated circuit.

23. A substrate-based assembly according to any one of the preceding claims which comprises at least one active optical component and at least one passive optical component.

24. A substrate-based assembly according to any one of the preceding claims having a substrate comprising at least one material from the group comprising silicon, glass, composite materials, ceramics and printed circuit board.

25. A substrate-based assembly according to any one of the preceding claims wherein the packaging layer is a passivation layer.

26. A substrate-based assembly according to any one of the preceding claims comprising at least two packaging layers, each of said at least two packaging layers comprising a glass material having both organic and inorganic components.

27. A substrate-based assembly according to Claim 26 wherein the refractive index of a first of the at least two packaging layers is different from the refractive index of a second of the at least two packaging layers.

28. A substrate-based assembly according to any one of the preceding claims wherein the packaging layer, or at least one packaging layer, transmits optical radiation in use of the assembly.

29. A substrate-based assembly according to any one of the preceding claims comprising at least one active optical component.

30. A substrate-based assembly according to Claim 29 wherein the active optical component comprises a laser or a tunable optical source.

31. A substrate-based assembly according to Claim 30, further comprising an optical modulator, external to the laser or tunable optical source.

32. A substrate-based assembly according to any one of the preceding claims wherein the substrate-based assembly comprises a thick substrate-based assembly.

33. A substrate-based assembly according to any one of the preceding claims wherein the substrate-based assembly has a thickness in the range from 1 micron to 1 millimetre.

34. Opto-electronic equipment comprising a substrate-based assembly according to any one of the preceding claims.

35. A method of packaging a substrate-based assembly, which method comprises the step of providing a packaging layer comprising a glass material having both organic and inorganic components.

36. A method of packaging a substrate-based assembly according to Claim 35, wherein the method further comprises the step of lithographic processing of the packaging layer.

37. A method of fabricating a substrate-based assembly, the assembly comprising at least one optical component mounted in relation to a substrate, the method comprising lithographic processing of each fabricated layer of the substrate-based assembly.

38. A method of fabricating a substrate-based assembly using bump bonding material to bump bond at least one optical component to a mounting pad, wherein the method comprises the steps of:

a) maintaining the temperature of the bump bonding material above a softening temperature for the material and micro-manipulating the component in relation to the mounting pad; and

b) lowering the temperature of the bump bonding material to below said softening temperature so as to achieve bump bonding.

39. A method of fabricating a substrate-based assembly comprising the step of using gray scale lithography to fabricate a groove of tapered cross section in a packaging layer for mounting a fibre for optical coupling with an optical component.

ABSTRACT

A packaging layer 200 for a wafer level assembly is fabricated from a glass material comprising both inorganic and organic components. This allows matching between the coefficient of thermal expansion of the packaging layer and that of other materials in the wafer assembly, particularly electrical interconnect materials. It is also possible to introduce properties to support such methods as photolithographic and low temperature processing of the packaging layer. This can improve fabrication accuracy and allows the packaging layer to be used with structures in a wafer assembly which might be damaged by high temperature processing, such as active optoelectronic devices and integrated circuits.

(Figure 11.)

FIGURE 1

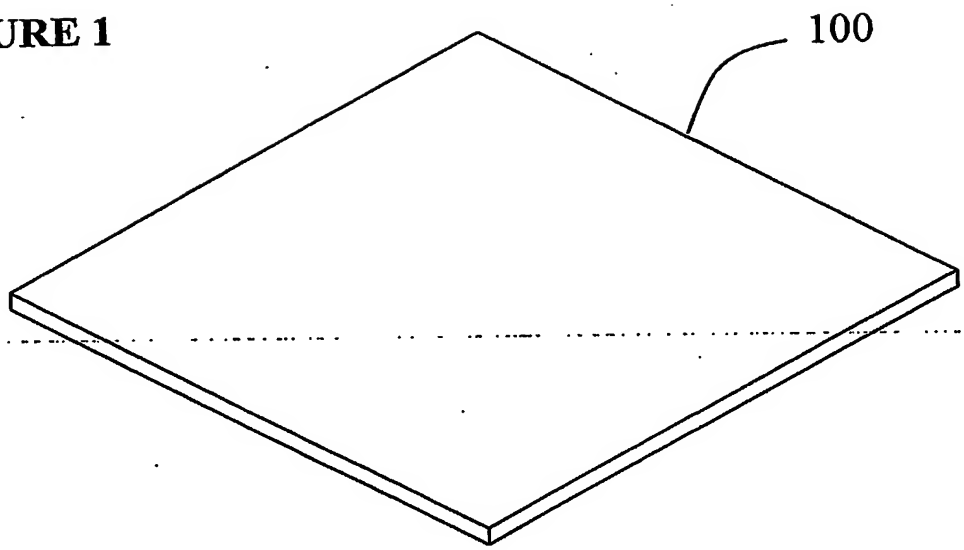


FIGURE 2

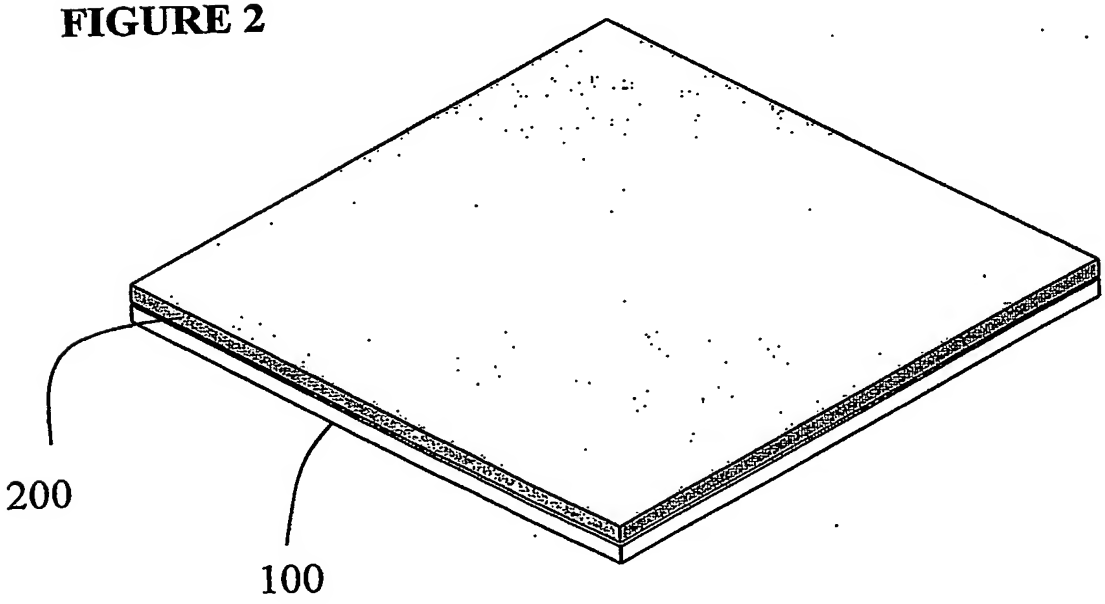


FIGURE 3

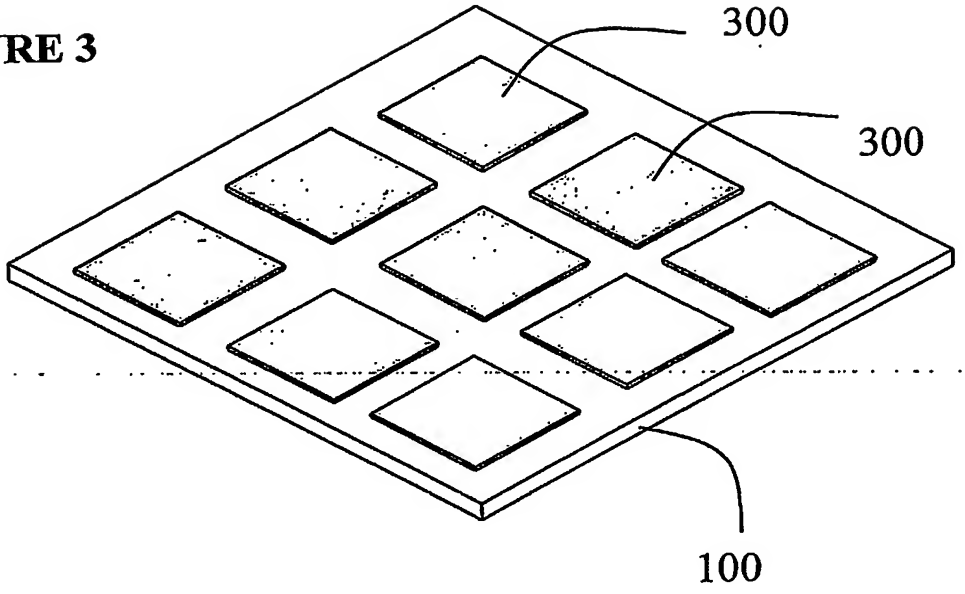


FIGURE 4

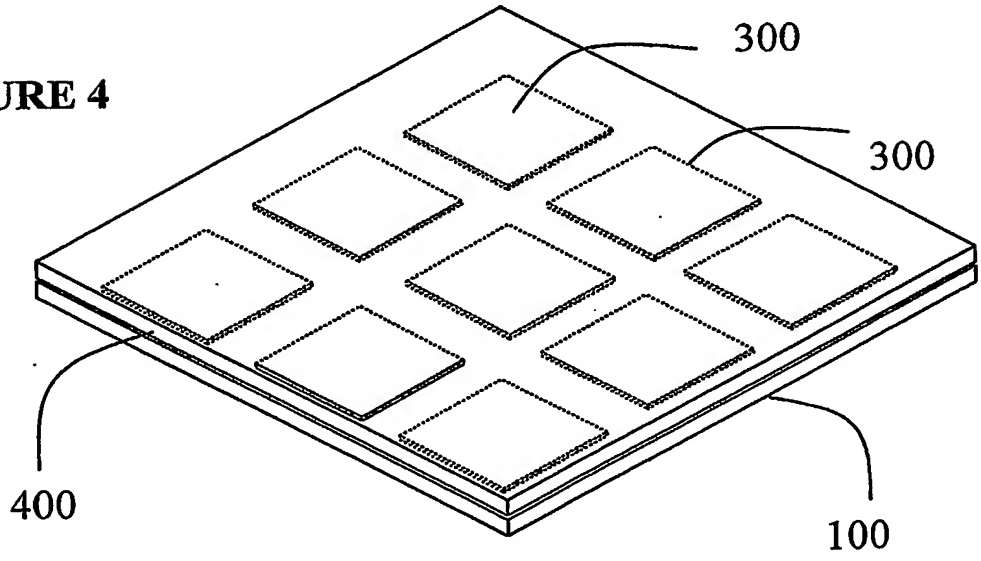


FIGURE 5

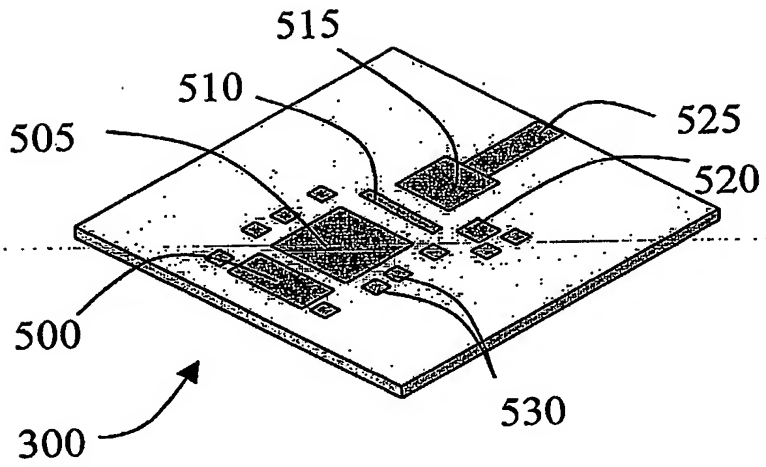


FIGURE 6

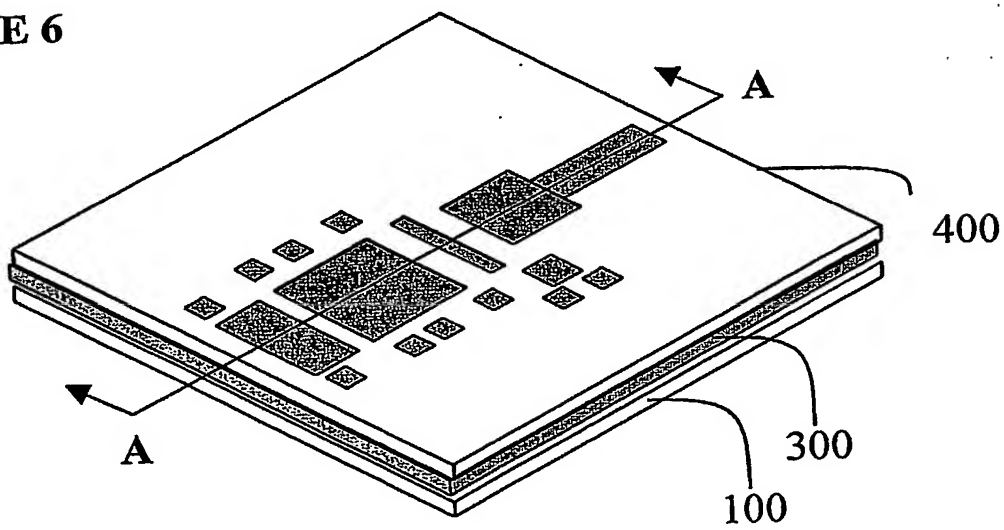


FIGURE 7

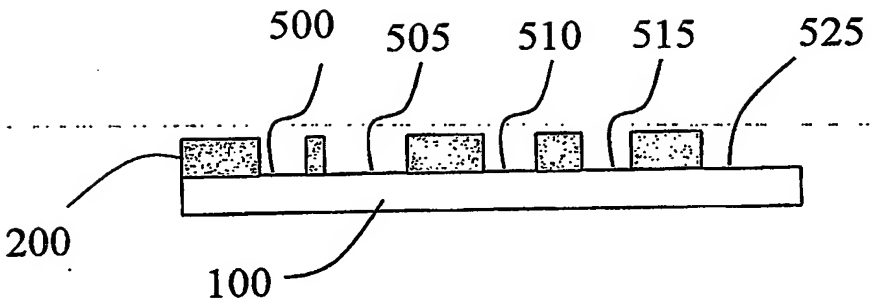


FIGURE 8

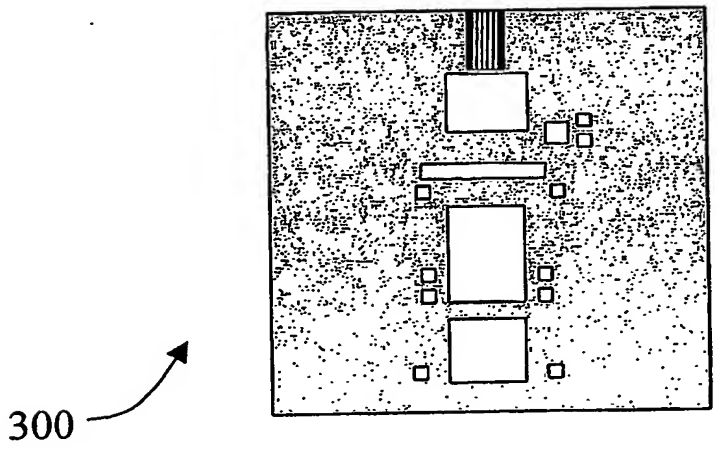


FIGURE 9

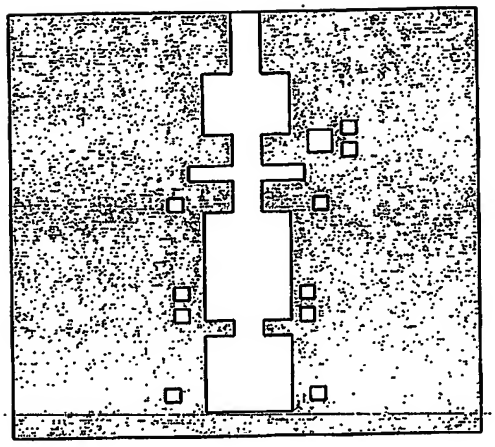


FIGURE 10A

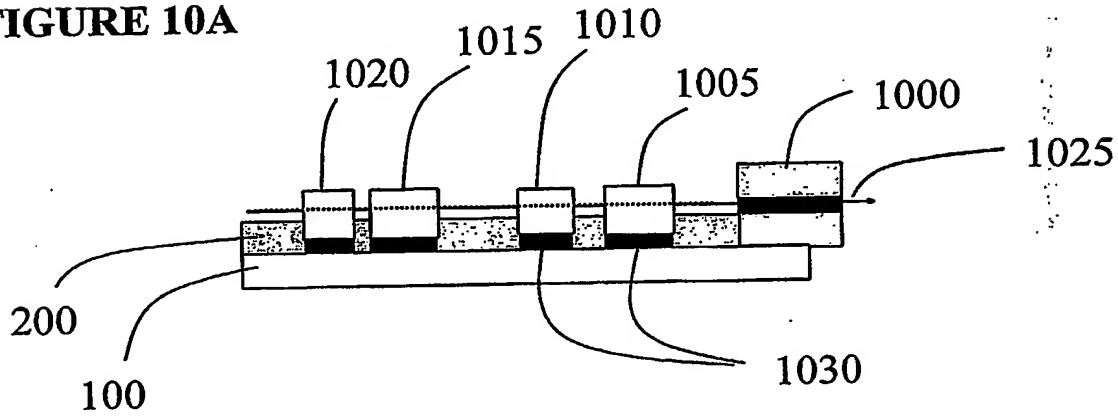
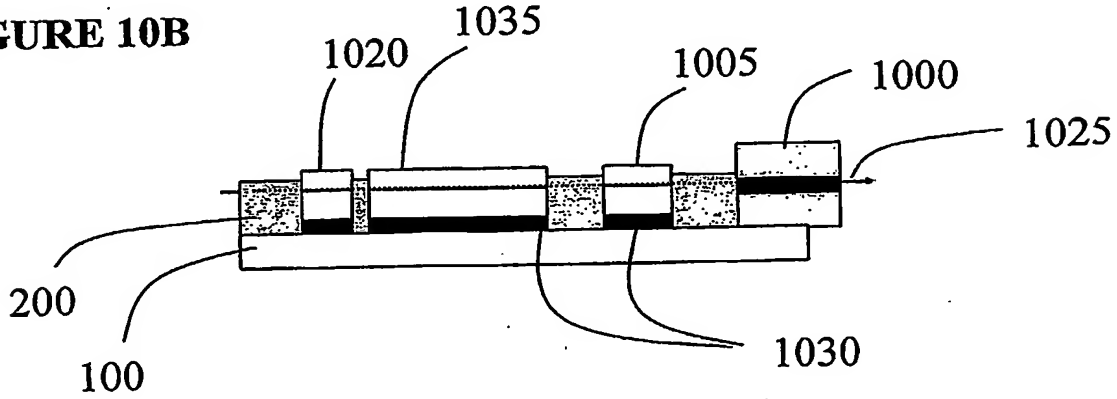


FIGURE 10B



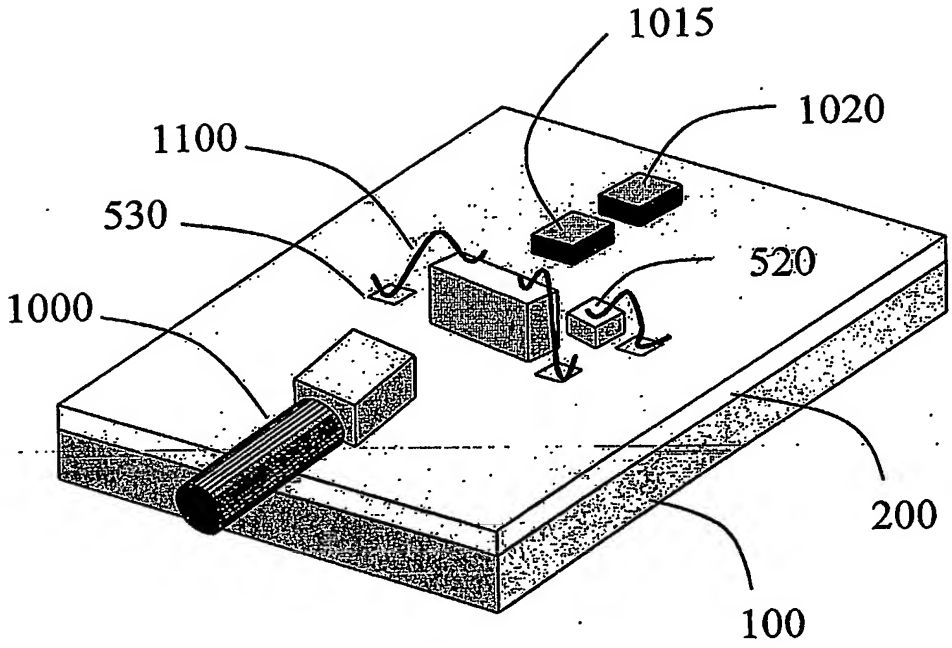


FIGURE 11

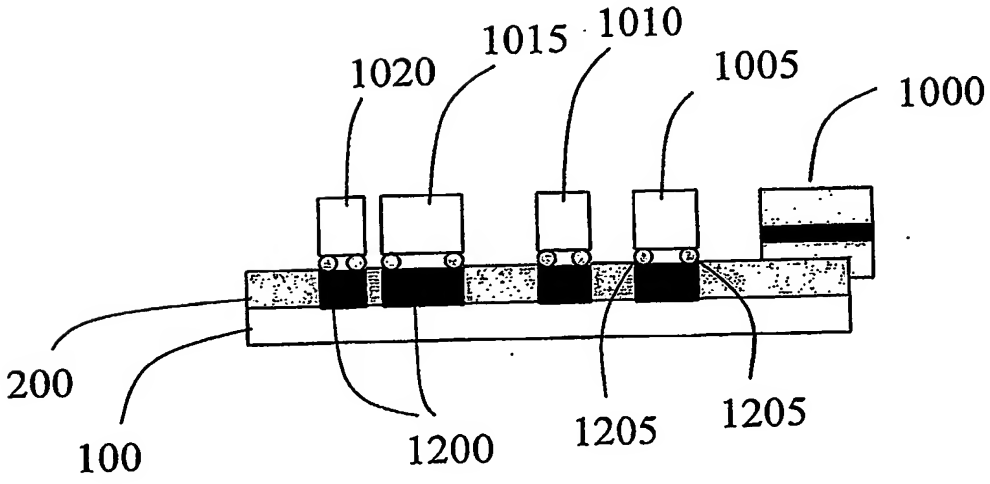


FIGURE 12

FIGURE 13

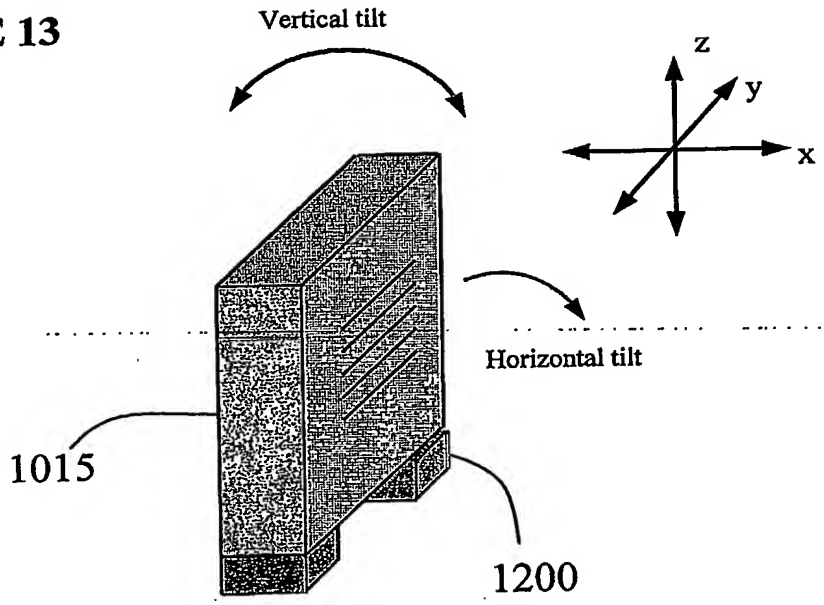


FIGURE 14

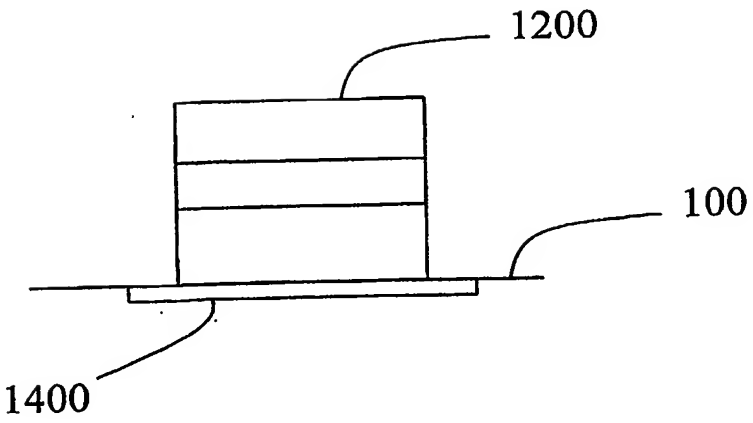


FIGURE 15